



ASSESSMENT and
QUALIFICATIONS
ALLIANCE

General Certificate of Education

Electronics 5431/6431

2008

Material accompanying this Specification

- Specimen and Past Papers and Mark Schemes
- Reports on the Examination
- Teachers' Guide

SPECIFICATION

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Background Information

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Advanced Subsidiary and Advanced Level Specifications

1.1 Advanced Subsidiary (AS)

Advanced Subsidiary courses were introduced in September 2000 for the award of the first qualification in August 2001. They may be used in one of two ways:

- as a final qualification, allowing candidates to broaden their studies and to defer decisions about specialism;
- as the first half (50%) of an Advanced Level qualification, which must be completed before an Advanced Level award can be made.

Advanced Subsidiary is designed to provide an appropriate assessment of knowledge, understanding and skills expected of candidates who have completed the first half of a full Advanced Level qualification. The level of demand of the AS examination is that expected of candidates half-way through a full A Level course of study.

1.2 Advanced Level (AS+A2)

The Advanced Level examination is in two parts:

- Advanced Subsidiary (AS) - 50% of the total award;
- a second examination, called A2 - 50% of the total award.

Most Advanced Subsidiary and Advanced Level courses are modular. The AS comprises three teaching and learning modules and the A2 comprises a further three teaching and learning modules. Each teaching and learning module is normally assessed through an associated assessment unit. The specification gives details of the relationship between the modules and assessment units.

With the two-part design of Advanced Level courses, centres may devise an assessment schedule to meet their own and candidates' needs. For example:

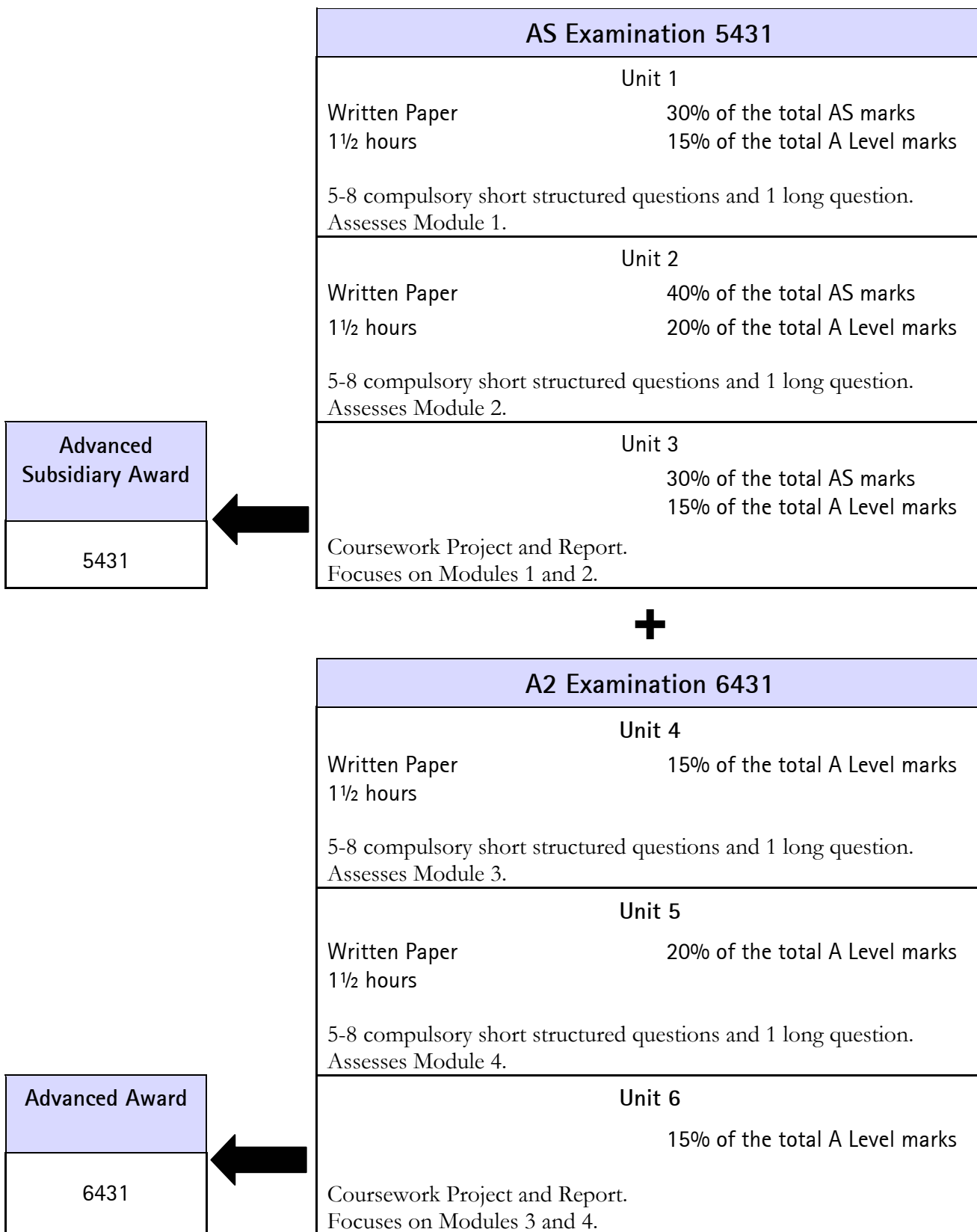
- assessment units may be taken at stages throughout the course, at the end of each year or at the end of the total course;
- AS may be completed at the end of one year and A2 by the end of the second year;
- AS and A2 may be completed at the end of the same year.

Details of the availability of the assessment units for each specification are provided in Section 3.

2

Specification at a Glance

Electronics



3

Availability of Assessment Units and Entry Details

3.1 Availability of Assessment Units

Examinations based on this specification are available as follows:

	Availability of Units		Availability of Qualification	
	AS	A2	AS	A Level
June	All	All	✓	✓

3.2 Sequencing of Units

It is recommended that Units 1, 2, 4 and 5 are taught in that sequence. Work for Unit 3 should be integrated with that for Units 1 and 2. Unit 6 work should be similarly integrated with that for Units 4 and 5.

3.3 Entry Codes

Normal entry requirements apply, but the following information should be noted.

The following unit entry codes should be used:

AS	A2
Unit 1 - ELE1	Unit 4 - ELE4
Unit 2 - ELE2	Unit 5 - ELE5
Unit 3 - ELE3	Unit 6 - ELE6

The **Subject Code** for entry to the AS only award is 5431

The **Subject Code** for entry to the Advanced Level award is 6431.

3.4 Classification Codes

Every specification is assigned to a national classification code indicating the subject area to which it belongs. Centres should be aware that candidates who enter for more than one GCE qualification with the same classification code, will have only one grade (the highest) counted for the purpose of the School and College Performance Tables.

The classification code for this specification is 1730.

3.5 Private Candidates

This specification is available to private candidates. Private candidates should write to the AQA for a copy of *'Supplementary Guidance for Private Candidates'*.

3.6 Access Arrangements and Special Consideration

AQA pays due regard to the provisions of the Disability Discrimination Act 1995 in its administration of this specification.

Arrangements may be made to enable candidates with disabilities or other difficulties to access the assessment. An example of an access arrangement is the production of a Braille paper for a candidate with a visual impairment. Special consideration may be requested for candidates whose work has been affected by illness or other exceptional circumstances.

Further details can be found in the Joint Council for Qualifications (JCQ) document:

Access Arrangements and Special Consideration

Regulations and Guidance Relating to Candidates who are Eligible for Adjustments in Examination

GCE, AEA, VCE, GCSE, GNVQ, Entry Level & Key Skills

This document can be viewed via the AQA Website (www.aqa.org.uk)

Applications for access arrangements and special consideration should be submitted to AQA by the Examinations Officer at the centre.

3.7 Language of Examinations

All Assessment Units in this subject are provided in English only.

Scheme of Assessment

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Rationale

Introduction

This GCE Electronics specification complies with

- the GCSE and GCE A/AS Code of Practice;
- the GCE Advanced Subsidiary and Advanced Level Qualification-Specific Criteria;
- the *Arrangements for the Statutory Regulation of External Qualifications in England, Wales and Northern Ireland: Common Criteria*.

The aim of this specification is to attract candidates to study Electronics and provide a rewarding and stimulating examination course. The inclusion of compulsory coursework will enable candidates to reach the full level of their individual potential.

Further, the specification also provides opportunities for students to develop the six Key Skills.

The general objectives of the specification are for candidates to:

- develop positive attitudes towards learning and applying Electronics principles
- develop ability and confidence in the subject
- develop an awareness of the importance of Electronics in society
- acquire a sound base of the knowledge, skills and attitudes required for further study in Electronics, in other subjects and in employment
- develop a rigorous approach to Electronics using the terms and techniques unique to the subject
- enable candidates to identify a problem, devise a specification for a solution and then implement it
- develop practical skills including those of dexterity, organisation and design.

Prior level of attainment And recommended prior learning

Candidates following AS/A Level courses in Electronics are expected to have achieved Grade C or above in GCSE Science (Double Award) or GCSE Science: Physics. It is not necessary for candidates to have studied GCSE Electronics before commencing work on this specification. The specification provides progression for entry to higher education and employment.

5

Aims

The specification aims to encourage candidates to:

- a. develop essential knowledge and understanding of concepts of Electronics, and where appropriate the applications of Electronics, and the skills needed for the use of these in new and changing situations;
- b. develop an understanding of the link between theory and practical work;
- c. sustain and develop their enjoyment of, and interest in Electronics;
- d. show the importance of Electronics as a human endeavour that has an impact on the relevance to social, economic and industrial matters;
- e. encourage candidates to develop skills in communication, application of number and information technology.

6

Assessment Objectives

Knowledge, understanding and skills are closely linked. Specifications should require that candidates demonstrate the following Assessment Objectives in the context of the content and skills prescribed.

At AS and A Level Candidates should be able to:

6.1 Knowledge with Understanding (A01)

- a. recognise, recall and show understanding of specific facts, theories, terminology, principles, relationships, conventions, concepts and practical techniques;
- b. draw on existing knowledge to show understanding of appropriate applications of Electronics and the ethical, social, economic, environmental and technological implications of Electronics-related applications;
- c. select, organise and present relevant information clearly and logically, using specialist vocabulary, spelling, punctuation and grammar with accuracy;
- d. describe the function, characteristics and mode of action of electronic components and devices;
- e. draw diagrams in a clear and logical fashion, using standard symbols and conventions.

- 6.2 Application of knowledge and understanding, synthesis and evaluation (A02)
- a. process, interpret and translate from one form to another, verbal, numerical and diagrammatic information;
 - b. demonstrate understanding of the operation of circuits in terms of the functions and properties of the passive and active devices involved;
 - c. apply systems principles in the analysis of functional devices;
 - d. design and evaluate systems against a given specification;
 - e. derive and use quantitative relationships in the analysis of circuits and gathered test data;
 - f. consider safety and maintenance requirements in the design circuits;
 - g. demonstrate an understanding of the relationships between different areas of the syllabus;
 - h. use and apply basic theories and concepts to solve problems in familiar and unfamiliar situations;
 - i. apply knowledge and understanding of Electronics to new situations including those which relate to the ethical, social, economic and technological implications and applications of Electronics.

- 6.3 Practical skills (A03)
- a. design and construct reliable circuits to perform specific functions;
 - b. investigate the behaviour and performance of devices, subsystems and systems;
 - c. apply safe and skilful working practices;
 - d. design appropriate test procedures to evaluate a circuit or system;
 - e. diagnose and locate faults in circuits and systems;
 - f. process, interpret, explain, evaluate and communicate the results of their project work.

At A level

- 6.4 Synthesis of knowledge, understanding and skills (A04)
- a. bring together principles and concepts from different areas of Electronics and apply in a particular context, expressing ideas clearly and logically and using appropriate specialist vocabulary;
 - b. use the skills of Electronics in contexts which bring together different areas of the subject.

- 6.5 Quality of Written Communication
- The quality of written communication is assessed in all assessment units where candidates are required to produce extended written material. Candidates will be assessed according to their ability to:
- select and use a form and style of writing appropriate to purpose and complex subject matter;
 - organise relevant information clearly and coherently, using specialist vocabulary when appropriate;
 - ensure text is legible, and spelling, grammar and punctuation are accurate, so that meaning is clear.

The assessment of the quality of written communication is included in Assessment Objective AO3.

7

Scheme of Assessment - Advanced Subsidiary (AS)

The Scheme of Assessment has a modular structure. The Advanced Subsidiary (AS) award comprises three compulsory assessment units.

7.1 Assessment Units

Unit 1 30% of the total AS marks	Written Paper 72 marks	1½ hours
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This unit comprises 5-8 short structured questions and 1 long question worth 18 marks. It assesses Module 1 of the AS Subject Content. All questions are compulsory.

Unit 2 40% of the total AS marks	Written Paper 72 marks	1½ hours
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This unit comprises 5-8 short structured questions and 1 long question worth 18 marks. It assesses Module 2 of the AS Subject Content. All questions are compulsory.

Unit 3 30% of the total AS marks	Coursework Project
--	---------------------------

This centre-assessed component requires candidates to complete a project and report.

7.2 Weighting of Assessment Objectives for AS

The approximate relationship between the relative percentage weighting of the Assessment Objectives (AOs) and the overall Scheme of Assessment is shown in the following table:

Assessment Objectives	Unit Weightings (%)			Overall Weighting of AOs (%)
	1	2	3	
Knowledge with understanding (AO1)	17	23	-	40
Application of knowledge and understanding, synthesis and evaluation (AO2)	13	17	-	30
Practical skills(AO3)	-	-	30	30
Overall Weighting of Units (%)	30	40	30	100

Candidates' marks for each assessment unit are scaled to achieve the correct weightings.

8

Scheme of Assessment - Advanced Level (AS+A2)

The Scheme of Assessment has a modular structure. The A Level award comprises three compulsory assessment units from the AS Scheme of Assessment and three compulsory assessment units from the A2 scheme of assessment.

8.1 AS Assessment Units

Unit 1 15% of the total A Level marks	Written Paper 72 marks	1½ hours
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Unit 2 20% of the total A Level marks	Written Paper 72marks	1½hours
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Unit 3 15% of the total A Level marks	Coursework Project 40 marks	
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8.2 A2 Assessment Units

Unit 4 15% of the total A Level marks	Written Paper 72 marks	1½ hours
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This unit comprises 5-8 short structured questions and 1 long question worth 18 marks. It assesses Module 3 of the A2 Subject Content. All questions are compulsory.

Unit 5 20% of the total A Level marks	Written Paper 72 marks	1½ hours
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This unit comprises 5-8 short structured questions and 1 long question worth 18 marks. It assesses Module 4 of the A2 Subject Content. All questions are compulsory.

Unit 6 15% of the total A Level marks	Coursework Project 40 marks	
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This centre-assessed component requires candidates to complete a project and report.

8.3 Synoptic Assessment

The Advanced Subsidiary and Advanced Level Criteria state that A Level specifications must include synoptic assessment (representing at least 20% of the total A Level marks). Units 4, 5 and 6 include synoptic assessment.

8.4 Weighting of Assessment Objectives for A Level

The approximate relationship between the relative percentage weighting of the Assessment Objectives (AOs) and the overall Scheme of Assessment is shown in the following table:

A Level Assessment Units (AS + A2)

Assessment Objectives	Unit Weightings (%)						Overall Weighting of AOs (%)
	1	2	3	4	5	6	
Knowledge with understanding (AO1)	8.5	11.5	-	4	6	-	30
Application of knowledge and understanding, synthesis and evaluation (AO2)	6.5	8.5	-	4	6	-	25
Practical skills(AO3)	-	-	15	-	-	10	25
Synthesis of knowledge, understanding and skills (AO4)	-	-	-	7	8	5	20
Overall Weighting of Units (%)	15	20	15	15	20	15	100

Candidates' marks for each assessment unit are scaled to achieve the correct weightings.

Subject Content

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Summary of Subject Content

9.1 AS Modules

MODULE 1 - Foundation Electronics

System synthesis
Logic gates and Boolean algebra
Current, voltage, power, resistance
Diodes
Resistive input transducers
Transistors and MOSFETs
Output devices
Operational amplifiers
Capacitors
RC networks (dc only)
555 timer circuit

MODULE 2 - Further Electronics

Design and simplification of combinational logic systems
Sequential logic systems
Counters
Operational amplifiers
Inverting amplifier
Non-inverting amplifier
Summing amplifier
Filter circuits
Power amplifiers

9.2 A2 Modules

MODULE 3 - Electronic Control Systems

General principles
Microprocessor control systems
Programming
Neural networks
Interfacing
Schmitt trigger circuits
Additional input and output devices

MODULE 4 - Communications Systems

General principles

Radio receivers

Mobile communication

Digital communication

Optoelectronics

10

AS Module 1

Foundation Electronics

Topic	Candidates should be able to:
10.1 System synthesis	<p>recognise that simple systems consist of an input, a process, an output and possibly feedback;</p> <p>analyse and design system diagrams;</p> <p>represent complex systems in terms of sub-systems;</p> <p>describe one modern electronic system which makes use of several sensors.</p>
10.2 Logic gates and Boolean algebra	
Introduction	<p>identify and use NOT, AND, OR, NAND, NOR and EX-OR gates in circuits;</p> <p>construct and recognise truth tables for these gates and simple combinations of gates with up to four inputs to the system;</p> <p>use combinations of these gates to form other logic functions;</p>
Boolean algebra	<p>generate the Boolean expression from a truth table or logic diagram.</p>
10.3 Current (I), voltage (V), power (P), resistance (R)	<p>understand the need for identifying a zero volt point in a circuit;</p> <p>define power as VI;</p> <p>define resistance as $\frac{V}{I}$;</p> <p>calculate the combined resistance of resistors connected in series and/or parallel;</p> <p>select appropriate preferred values from the E24 series;</p> <p>identify resistors using the colour code and BS 1852 code.</p>
10.4 Diodes	
Light emitting diodes	<p>sketch and interpret $I-V$ characteristic curves of LEDs and calculate the value of the series resistor for dc circuits;</p>
Silicon diodes and zener diodes	<p>sketch $I-V$ characteristics for silicon diodes and zener diodes;</p> <p>select appropriate silicon diodes and zener diodes from given data sheets;</p> <p>describe how a zener diode can be used with a current limiting resistor to form a simple regulated voltage supply;</p> <p>calculate the value of a suitable current limiting resistor.</p>

10.5 Resistive input transducers	interpret and use characteristic curves;
Light dependent resistors, thermistors and variable resistors	describe the use of LDRs and negative temperature coefficient thermistors in a voltage dividing chain to provide analogue signals;
Voltage dividers	calculate suitable values for series resistors for use with and for protection of LDRs and thermistors; perform calculations on voltage dividers consisting of resistors and devices described above.
<hr/>	
10.6 Transistors and MOSFETs	
<i>npn</i> junction transistor	describe its use as a switch;
n-channel (enhancement mode) MOSFETs	describe its use as a switch; compare the advantages and disadvantages of a MOSFET with a junction transistor when both are used as switch.
<hr/>	
10.7 Output devices	
Electromagnetic relays, solenoids, buzzers and motors	describe their use, but not construction details; understand and explain circuit protection provided by a diode in parallel with a relay; understand and use NO and NC notation.
<hr/>	
10.8 Operational amplifiers	
General properties	know the characteristics of an ideal op-amp and be aware that the characteristics of a typical op-amp may be different; know the difference between inverting and non-inverting inputs; understand power supply requirements and output voltage swing limitations of real op-amps leading to saturation;
The op-amp as a voltage comparator	understand and explain the use of an op-amp in a comparator circuit.
<hr/>	
10.9 Capacitors	understand that a capacitor, whether isolated or as part of a circuit, is capable of storing electrical charge and energy; realise that the farad is a large unit and that practical capacitors are usually measured in pF, nF or μF ; calculate the combined capacitance of capacitors connected in series and/or parallel; select appropriate capacitors given data on maximum working voltage, temperature coefficient, polarisation and leakage current.

10.10 RC networks (dc only)

understand the meaning of and calculate the value of the time constant for RC circuits;

know that after one time constant:

$$V = 0.63V_s \text{ for a charging capacitor,}$$

$V = 0.37V_s$ for a discharging capacitor, where V_s is the supply voltage and V is the voltage across the capacitor;

know that:

$$V = 0.5V_s \text{ after time } 0.69RC,$$

$$V \approx V_s \text{ after time } 5RC \text{ for a charging capacitor,}$$

$$V \approx 0 \text{ after } 5RC \text{ for a discharging capacitor;}$$

sketch voltage/time graphs for charging and discharging.

10.11 555 timer circuit**555 monostable circuit**

draw, recognise and use the circuit diagram for a 555 monostable, treating it as a functional block;

calculate its time period using $T = 1.1 RC$;

555 astable circuit

draw, recognise and use the circuit diagram for a 555 astable, treating it as a functional block;

calculate frequency using $f = \frac{1.44}{(R_A + 2R_B)C}$;

calculate the time that the output is low (t_L) using

$$t_L = 0.7 R_B C ;$$

calculate the time that the output is high (t_H) using

$$t_H = 0.7 (R_A + R_B)C.$$

AS Module 2

Further Electronics

Topic

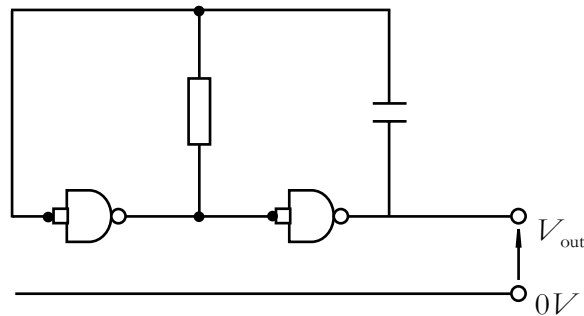
Candidates should be able to:

11.1 Design and simplification of combinational logic systems

design a logic system from a truth table or description using combinations of gates;
 simplify logic systems using either Boolean algebra or Karnaugh maps;
 convert logic systems comprising mixed gates into NOR or NAND gates only;
 explain the operation of combinational logic systems.

11.2 Sequential logic systems

draw a bistable latch based on NAND gates and describe its function;
 draw the symbol for a D-type flip-flop and describe its function;
 describe the use of D-type flip-flops to make a shift register;
 explain the operation of monostable circuits based on NAND gates and estimate the time period using $T \approx RC$;
 explain the operation of an astable circuit based on NAND gates and estimate the operating frequency using $f \approx \frac{1}{2RC}$



11.3 Counters

describe the use of feedback to make a D-type flip-flop divide by 2;
 convert a 4-bit binary number to decimal or HEX notation;
 design 4-bit up or down counters based on rising edge triggered D-type flip-flops;
 design 4-bit modulo-N counters and draw timing diagrams for these counters;
 describe the use of a BCD or HEX decoder with a seven-segment display.

11.4 Operational Amplifiers

define the bandwidth of an amplifier as the frequency range over which the voltage gain is within 70% of maximum;

know that for a real op-amp system the product *gain* × *bandwidth* is constant;

use the equation voltage gain = $\frac{V_{\text{out}}}{V_{\text{in}}}$

11.5 Inverting amplifier

draw and recognise the inverting amplifier circuit and describe its applications;

use the formula $\frac{V_{\text{out}}}{V_{\text{in}}} = -\frac{R_f}{R_1}$

know that the input resistance is equal to the value of the input resistor.

11.6 Non-inverting amplifier

draw and recognise the non-inverting amplifier circuit;

use the formula voltage gain = $1 + \frac{R_f}{R_1}$

know that the input resistance is equal to that of the op-amp;

draw and recognise a voltage follower (buffer) based on a non-inverting op-amp;

show that the voltage follower has a gain of 1;

describe and explain a use for the voltage follower;

describe the effects of negative and positive feedback in op-amp circuits.

11.7 Summing amplifier

draw and recognise a summing amplifier circuit;

describe and explain applications, including mixing audio signals and digital to analogue conversion;

calculate resistor values for the above applications;

use the formula

$$V_{\text{out}} = -R_f \left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \right)$$

11.8 Filter circuits

calculate the reactance of a capacitor using the formula

$$X_c = \frac{1}{2\pi fC}$$

draw and explain passive filters using RC circuits;

draw and explain first order active filters including treble cut, treble boost, bass cut and bass boost;

calculate the break point of active filter circuits.

11.9 Power amplifiers

- describe and recognise a source follower as a power amplifier;
- draw circuits for push-pull output circuits using p- and n- channel enhancement mode MOSFETs;
- explain the operation of push-pull output circuits;
- explain crossover distortion and describe how it can be reduced;
- describe the advantages of push-pull output circuits over single ended output circuits;
- estimate the maximum power output from a push-pull circuit;
- calculate the power dissipated in a transistor and select an appropriate heat sink;
- explain the features of heat sinks which make them efficient.

12

A2 Module 3

Electronic Control Systems

Topic

Candidates should be able to:

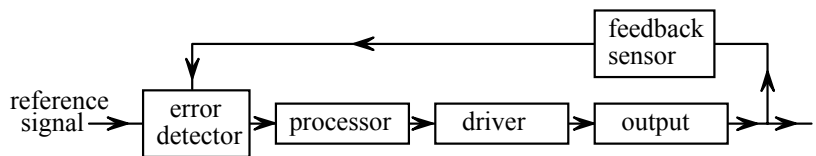
12.1 General principles

distinguish between open loop and closed loop control systems and discuss their characteristics;

describe what is meant by feedback in a control system, and give examples of systems with feedback;

distinguish between positive and negative feedback in control systems and discuss the characteristic effects of each;

describe the features of the generalised control system, shown below:



12.2 Microprocessor control systems

distinguish between and discuss the relative merits of hardwired systems and software controlled systems;

describe the architecture of a generalised microprocessor control system consisting of microprocessor, clock, memory (ROM and RAM) and input/output ports, connected by databus, address bus and control bus;

explain what is meant by memory mapping and I/O mapping;

describe the architecture of a basic single chip microprocessor systems, eg PIC or AVR devices;

describe the social and economic implications of the use of single chip microprocessor systems, e.g. PIC or AVR devices.

12.3 Programming

design and interpret flow charts to read data from input devices and to control the operation of output devices;

convert a flowchart into a program written in Basic to:

read data from a sensor,

create a specified time delay,

create a specified sequence of control signals,

perform simple arithmetic and logic operations,

write data to an output device,

use polling to detect events;

compare the use of hardware interrupts and polling to trigger events;

interpret programs written in Basic.

12.4 Neural networks

describe the basic principle of a neural network;

describe an example of a system that uses or could use a neural network;

explain the advantages and disadvantages of the use of microprocessor systems that can be 'trained';

describe the social, economic and cultural impact of the increasing use of neural network systems.

12.5 Interfacing

describe the use of tri-state buffers;

describe the use of data latches;

describe the operation of and use of a Centronics type port on a microprocessor system;

describe the use of an 8-bit DAC based on a summing amplifier;

draw a block diagram for an 8-bit digital ramp ADC and explain how it works, including timing diagrams for the system;

describe the circuit for a flash ADC and explain how it works;

describe how an ADC and DAC would be connected to a microprocessor system, including timing diagrams for the control signals;

compare and explain the relative merits of flash ADCs and digital ramp ADC.

12.6 Schmitt trigger circuits

know the function of Schmitt trigger circuits;

draw and recognise both inverting and non-inverting Schmitt trigger circuits and calculate trigger levels.

12.7 Additional input and output devices

describe and explain the use of:

- an optical shaft encoder,
- a photodiode / opto-switch;

describe and explain the use of:

- a stepper motor,
- seven segment and dot matrix LED displays;

explain why signal conditioning is often needed for input transducers, and how a Schmitt trigger circuit can be used to provide it.

13

A2 Module 4

Communications Systems

Topic	Candidates should be able to:
<p>13.1 General principles</p>	<p>know that communication is the transfer of meaningful information from one location to another;</p> <p>draw a block diagram of a generalised communications system, consisting of input transducer, carrier generator, modulator/encoder, transmitter, transmission link (medium), receiver, demodulator/decoder, output transducer;</p> <p>compare in qualitative terms the transmission of electromagnetic signals along conducting cable, optical fibre, and in free space;</p> <p>understand the relationship between bandwidth and capacity to carry information;</p> <p>understand the need to multiplex a number of signals onto one transmission medium;</p> <p>describe the principles of frequency division multiplexing and time division multiplexing;</p> <p>distinguish between noise, distortion and crosstalk;</p> <p>calculate and appreciate the significance of signal-to-noise ratio (in dB).</p>
<p>13.2 Radio receivers</p> <p>Modulation</p>	<p>understand the need for a carrier wave;</p> <p>explain how the signal amplitude and frequency are encoded on the carrier using amplitude modulation (AM);</p> <p>draw time waveforms to illustrate the nature of AM including the effect of depth of modulation on the envelope;</p> <p>draw and label a frequency spectrum for a sinusoidal carrier amplitude modulated by:</p> <ul style="list-style-type: none"> a single frequency signal, showing the carrier and side frequencies a signal consisting of a range of frequencies, showing the carrier and sidebands; <p>describe the bandwidth requirements of AM signals;</p> <p>explain how the signal's amplitude and frequency are encoded on the carrier using frequency modulation (FM);</p> <p>draw time waveforms to illustrate the nature of FM;</p> <p>describe the bandwidth requirements of FM signals.</p>

Channel spacing and signal bandwidth	<p>Know that radio stations broadcasting in LF and MF bands use AM;</p> <p>Describe channel allocation within LF and MF broadcasting;</p> <p>Know that FM is used for entertainment broadcasting in the VHF band;</p> <p>Understand the relationship between channel spacing and signal bandwidth.</p>
Simple receiver	<p>Draw a block diagram for a simple radio receiver, consisting of antenna, tuned circuit, detector/demodulator and output device;</p> <p>Calculate the optimum length for a half-wave dipole for a given wavelength/frequency;</p> <p>Know that the impedance of the antenna should match that of the feed.</p>
Resonance and tuned circuits	<p>Describe in qualitative terms, how voltage and current vary in a parallel LC circuit near resonance;</p> <p>Know that resonance occurs when $X_L = X_C$ and hence calculate the resonant frequency;</p> <p>Draw a resonance curve for a parallel LC circuit;</p> <p>Describe and explain the use of a LC network to select a particular frequency;</p> <p>Explain the significance of the quality factor of a tuned circuit and its relationship to the selectivity of the receiver;</p> <p>use the resonant frequency formula to calculate suitable values of L and C ;</p> <p>Describe how an rf amplifier can be used to improve sensitivity.</p>
Superhet receiver	<p>Draw a block diagram for a superhet receiver consisting of antenna, rf amplifier, local oscillator, mixer, if amplifier and filter, demodulator, AGC, af amplifier and loudspeaker;</p> <p>Describe the principle of operation of the superhet;</p> <p>Describe the frequency spectrum at the output of the mixer;</p> <p>Describe the advantages of the superhet receiver over a simple receiver.</p>

13.3 Mobile communications

Understand that mobile telephones are connected to the main telephone network via a radio link to a nearby base station;

Understand and explain how a large number of mobile telephones can be used within a restricted frequency allocation;

Calculate the maximum number of mobile telephones that can be supported on one cell given the size of the cell and the available bandwidth;

Understand and explain the meaning of the following terms: repeater, regenerator, cellular, frequency reuse;

State and describe any situation in which mobile communications can affect everyday life.

13.4 Digital communication	compare the relative merits of analogue and digital communication;
Pulse modulation	describe and illustrate the following pulse modulation techniques: <ul style="list-style-type: none"> pulse amplitude modulation (PAM) pulse width modulation (PWM) pulse position modulation (PPM) pulse code modulation (PCM) <p>explain how the sampling rate affects the bandwidth of the digital signal and be able to perform appropriate calculations.</p>
Serial transmission	describe and discuss the relative merits of half and full duplex communication links; <p>describe and discuss the relative merits of serial and parallel data transmission;</p> <p>describe and discuss the relative merits of synchronous and asynchronous transmission;</p> <p>describe the use of start and stop bits, and a parity bit;</p> <p>calculate bit and baud rate.</p>
Shift registers	describe the use of serial and parallel shift registers and draw their timing diagrams.
Multiplexers	describe the action of a multiplexer; <p>describe the use of multiplexers for serial data transmission;</p> <p>design a logic diagram for a 4 to 1 multiplexer.</p>

13.5 Optoelectronics	describe and explain the use of glass in an optical fibre; <p>understand and explain the use of total internal reflection in optical fibre systems;</p> <p>describe the effect of attenuation and dispersion on an optical digital signal;</p> <p>explain the use of laser diodes as light sources;</p> <p>explain the use of avalanche photodiodes as detectors (detailed knowledge of devices not required);</p> <p>describe and compare optical fibre and wired systems in particular situations.</p>
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Key Skills and Other Issues

14

Key Skills – Teaching, Developing and Providing Opportunities for Generating Evidence

14.1 Introduction

The Key Skills Qualification requires candidates to demonstrate levels of achievement in the Key Skills of *Application of Number*, *Communication* and *Information Technology*.

The units for the wider Key Skills of *Improving own Learning and Performance*, *Working with Others* and *Problem-Solving* are also available. The acquisition and demonstration of ability in these ‘wider’ Key Skills is deemed highly desirable for all candidates, but they do not form part of the Key Skills Qualification. Copies of the Key Skills Units may be downloaded from QCA Website (www.qca.org.uk/keyskills)

The units for each Key Skill comprise three sections:

- A. What you need to know.
- B. What you must do.
- C. Guidance.

Candidates following a course of study based on this specification for Electronics can be offered opportunities to develop and generate evidence of attainment in aspects of Communication, Application of Number, Information Technology, Improving own Learning, Working with Others and Problem-Solving. Areas of study and learning that can be used to encourage the acquisition and use of Key Skills, and to provide opportunities to generate evidence for Part B of the units, are signposted below. More specific guidance on integrating the delivery of Key Skills in courses based upon this specification is given in the AQA specification support material.

14.2 Key Skills Opportunities in Electronics

The broad and multi-disciplinary nature of Electronics, that calls upon candidates’ abilities to demonstrate the transferability of their knowledge, understanding and skills, make it an ideal vehicle to assist candidates to develop their knowledge and understanding of the Key Skills and to produce evidence of their application. The matrices below signpost the opportunities for the acquisition, development and production of evidence for Part B of the six Key Skills units at *Level 3*, in the teaching and learning modules of this specification. The degree of opportunity in any one module will depend upon a number of centre-specific factors, including teaching strategies and level of resources.

Communication

What you must do:	Signposting of Opportunities for Generating Evidence in Modules					
	1	2	3	4	5	6
C3.1a Contribute to discussions	✓	✓	✓	✓	✓	✓
C3.1b Make a presentation	✓	✓	✓	✓	✓	✓
C3.2 Read and synthesise information	✓	✓	✓	✓	✓	✓
C3.3 Write different types of documents	✓	✓	✓	✓	✓	✓

Application of Number

What you must do:	Signposting of Opportunities for Generating Evidence in Modules					
	1	2	3	4	5	6
N3.1 Plan and interpret information from different sources	✓	✓	✓	✓	✓	✓
N3.2 Carry out multi-stage calculations	✓	✓	✓	✓	✓	✓
N3.3 Present findings, explain results and justify choice of methods	✓	✓	✓	✓	✓	✓

Information Technology

What you must do:	Signposting of Opportunities for Generating Evidence in Modules					
	1	2	3	4	5	6
IT3.1 Plan and use different sources to search for and select information	✓	✓	✓	✓	✓	✓
IT3.2 Explore, develop and exchange information, and derive new information	✓	✓	✓	✓	✓	✓
IT3.3 Present information including text, numbers and images			✓			✓

Working with Others

What you must do:	Signposting of Opportunities for Generating Evidence in Modules					
	1	2	3	4	5	6
WO3.1 Plan the activity	✓	✓		✓	✓	
WO3.2 Work towards agreed objectives	✓	✓		✓	✓	
WO3.3 Review the activity	✓	✓		✓	✓	

Improving own Learning and Performance

What you must do:	Signposting of Opportunities for Generating Evidence in Modules					
	1	2	3	4	5	6
LP3.1 Agree and plan targets			✓			✓
LP3.2 Seek feedback and support			✓			✓
LP3.3 Review progress			✓			✓

Problem-Solving

What you must do:	Signposting of Opportunities for Generating Evidence in Modules					
	1	2	3	4	5	6
PS3.1 Recognise, explain and describe the problem			✓			✓
PS3.2 Generate and compare different ways of solving problems			✓			✓
PS3.3 Plan and implement options			✓			✓
PS3.4 Agree and review approaches to tackling problems			✓			✓

NB. The signposting opportunities recorded in the six tables above, represent the opportunities to acquire, and produce evidence of the Key Skills which are possible through this specification. There may be other opportunities to achieve these and other aspects of Key Skills via this specification, but such opportunities are dependent on the detailed course of study delivered within centres.

14.3 Key Skills in the Assessment of Electronics

The Key Skills of *Application of Number* and *Communication* must contribute to the assessment of Electronics. *Communication* is an intrinsic part of Assessment Objective 3. Aspects of *Application of Number* will form an intrinsic part of the assessment requirements for all modules. Both Key Skills will form part of the assessment requirements for Units 1, 2, 3, 4, 5, 6.

14.4 Further Guidance

More specific guidance and examples of tasks that can provide evidence of single Key Skills or composite tasks that can provide evidence of more than one Key Skill are given in the AQA specification support material.

Moral, Ethical, Social, Cultural and Other Issues

15.1 Moral, Ethical, Social and Cultural Issues

It is clear that Electronics plays a major part in modern world development whether this be in the form of the domestic personal computer or the impact of global communication. This specification is keenly aware of the implications of this development. The general philosophy of the subject is rooted in an ethical approach. In particular, there are references in the specification to the social, economic, moral and cultural effects of electronic aspects of technological advance.

The following sections of the specification may be particularly apposite for analysis and discussion of moral and cultural issues:

- the social and economic implications of the use of single chip microprocessor systems (12.2)
- the advantages and disadvantages of the use of microprocessor systems that can be ‘trained’ (12.4)
- the social, economic and cultural impact of the increasing use of neural network systems (12.4)
- general principles of communications systems and efficient use of bandwidth (13.1)
- awareness of the implications of the use of mobile communications (13.3)

15.2 European Dimension

AQA has taken account of the 1988 Resolution of the Council of the European Community in preparing this specification and associated specimen papers. The specification is designed to improve candidates’ knowledge and understanding of the international debates surrounding new technology and to foster responsible attitudes to them. (See Section 12.2 and 12.4)

Students need to be aware of EU regulations regarding electromagnetic comparability of equipment (EMC) and software legislation in relation to copyright.

15.3 Environmental Education

AQA has taken account of the 1988 Resolution of the Council of the European Community and the Report *“Environmental Responsibility: An Agenda for Further and Higher Education”* 1993 in preparing this specification and associated specimen papers. The specification is designed to improve candidates’ awareness of environmental matters though consideration of the impact of electronic systems.

15.4 Avoidance of Bias

AQA has taken great care in the preparation of this specification and associated specimen papers to avoid bias of any kind.

15.5 Data Sheet

Each candidate will be supplied with a data sheet (see Appendix B) for use in written examinations.

15.6 Mathematical Requirements

Students should have a knowledge and understanding of Mathematics defined in the National Curriculum, up to and including level 7 in the relevant attainment targets. In addition, knowledge of the following topics will be assumed.

Logarithms: to base 10 and base e ; decibels.

Graphical representations: interpretation of slope and areas when these have physical significance; graphs involving logarithmic and semi-logarithmic scales and quantities such as the decibel.

Sine and cosine waves: knowledge of form, amplitude, frequency and phase (measured in degrees).

Exponentials: qualitative description of exponential decay; attenuation and charging/discharging in CR and LR circuits.

Number systems: binary and hexadecimal.

Standard notation: use of standard notation; significant figures and tolerances; negative index notation for units.

It is assumed that candidates will have the use of calculators which have at least the functions of addition (+), subtraction (-), multiplication (\times), division (\div), square root ($\sqrt{\quad}$), sine, cosine, tangent, natural logarithms and their inverses and a memory.

15.7 Health and Safety

Candidates should make every effort to make themselves aware of any safety hazards involved in their work. As part of their coursework they will be expected to undertake risk assessments to ensure the safety of themselves, associated workers, the components and test equipment.

Centre-Assessed Component

16

Nature of Centre-Assessed Component

Within the scheme of assessment, the coursework unit (Unit 3) will contribute 30% to the AS award as a whole. In the case of A level, the coursework units (Units 3 and 6) will contribute 30% to the award as a whole.

The coursework undertaken by the candidates for each of the units will be to design and construct a single artefact to satisfy an initial design problem identified by the candidate. The work for each coursework unit is expected to be an independent piece of work carried out alongside the theoretical studies of the candidates. The aim for the candidate is to design, assemble and evaluate an electronic artefact and produce a written report of the work.

16.1 Relationship of Coursework Skills to Assessment Objectives

Practical Skills	AS	A2	Total in A Level
AO3	30%	20%	25%

16.2 Subject Content

Coursework for AS should be based on the Subject Content for AS. Coursework for A2 should be based on the A2 Subject Content.

Guidance for Setting Centre-Assessed Component

The AS coursework undertaken for Unit 3 should be such that it can be completed in 30 hours and should be based on at least three active devices. The level and content of the coursework should be commensurate with the content of Module 1 and Module 2.

Candidates should be encouraged to select projects in which they are interested and which are considered achievable.

The A2 coursework undertaken for Unit 6 should be such that it can be completed in 30 hours. It is expected that this will be of a more demanding nature than the work for Unit 3 and should reflect the content of the A2 syllabus. Candidates should be encouraged to select projects in which they are interested and which are considered achievable. Teachers should also ensure that the work undertaken is both of an appropriate standard and within the capability of the candidate.

Having decided upon the aim of the project the candidates should undertake appropriate research so that a list of performance parameters (Specification) can be given. It is expected that the specification will contain realistic numerical values against which the final performance of the work can be judged. Candidates are expected to consider alternatives and give reasons for selecting the chosen solution.

The overall system for each module should be developed as sub-systems which should be tested and evaluated in isolation before being incorporated into the complete system. This will ensure that the complete system grows by a gradual and incremental process, having been assessed at each stage of its development.

Candidates will be expected to develop their coursework systems on protoboard and may use computer simulations to help them. The systems can be left in protoboard form; there is no requirement for candidates to transfer their work to strip board or printed circuit board. For all modes of circuit, the layout and mounting of components, section and wiring should be neat and logical in order to assist in the design, testing and fault finding processes. Candidates will be expected to undertake Risk Assessments during their coursework in order to ensure the safety of themselves, associated workers, the components and test equipment.

When the project is completed, testing of the complete system should take place but only for the conditions likely to be encountered in normal operation. It should not be tested to destruction. The testing should be fully documented with results being displayed in tables and graphs as appropriate. These tests will enable the candidate to assess the system and identify faults and limitations. The candidate should aim to modify the final system to correct for any limitations and then produce a final set of performance figures for the completed system. The candidate should then evaluate the final system against the initial specification and so recommend possible further developments.

Centres must assure AQA that the assessment submitted are the work of the candidates concerned. As much coursework as possible must be undertaken under the direct supervision of teachers.

The teacher responsible for the supervision of the candidates' work must complete a Centre Declaration Sheet (Appendix C) to certify that the marks submitted were awarded in accordance with the syllabus and Instructions and Guidance on Coursework and that he/she is entirely satisfied that the work submitted is that of the candidate concerned.

It is perfectly acceptable for parts of a candidate's coursework to be adapted from other sources so long as all such cases are clearly identified in the text and fully acknowledge either on the Candidate Record Form (Appendix C) or in the supporting evidence. Where candidates quote directly from a source, e.g. circuit diagrams or sentences, quotation marks should be used and the reference provided in a foot note at the bottom of the page.

Assessment Criteria

18.1 Introduction

Marks should be awarded for the skills listed below in paragraph 18.2 for both the AS and A2 coursework. Standards are set by the use of mark criteria which describe the performance expected for a particular mark.

18.2 Criteria

Marks should only be awarded when there is clear supporting evidence.

The assessment criteria below are not hierarchical; each statement satisfied gains a mark. Those criteria marked with * contribute to synoptic assessment.

A. Aim

The candidate:

- a. defined the problem to be solved with minimal guidance.

B. Research

The candidate:

- a. carried out research from two or more named sources
- b. carried out investigations of two or more relevant factors.

C. Specification

The candidate:

- a. gave a detailed description of the system requirements specifying at least one parameter
- b. specified at least one numerical parameter
- c. specified numerically and realistically three or more parameters.

D. Generation of possible solutions

The candidate:

- a. considered more than one solution in outline*
- b. gave some reasons for the choice of solution.*

E. Sub-system development

The candidate:

- a. developed the system using sub-systems *
- b. performed at least one relevant calculation on a sub-system*
- c. devised circuit details of at least one sub-system with minimal guidance*
- d. made and recorded measurements on at least one sub-system*
- e. assessed and documented clearly the performance of at least one sub-system*
- f. considered the interfacing between sub-systems.*

F. System Details

The candidate:

- a. gave a clear description of how the system works *
- b. gave a clear and detailed description of how the complete system works *
- c. performed at least one relevant calculation on the complete system.*

- G. Component Layout The candidate:
- produced a circuit board layout
 - produced a well organised circuit board layout with minimal guidance.
- H. Construction The candidate:
- worked safely at all times
 - constructed two or more subsystems of the complete electronic system
 - produced a neat and well organised electronic system
 - made part of the system function
 - made most of the system function
 - made all of the system function with minimal guidance.
- I. Testing the system The candidate:
- devised an appropriate test procedure for the complete system
 - devised a full and appropriate test procedure with minimal guidance for the complete system.
- J. Measurements The candidate:
- made and recorded basic numerical measurements on the complete system
 - made and recorded detailed numerical measurements on the complete system
 - made and recorded all reasonable numerical measurements on the complete system.
- K. Assessing The candidate:
- made some assessment of the overall performance of the complete system
 - assessed the working parts of the complete system and referred to the measurements made.
- L. Limitations and Modifications The candidate:
- identified some limitations in the performance of the complete system *
 - suggested modifications to overcome the limitations in the performance of the complete system *
 - carried out the modifications. *
- M. Evaluation of Final System The candidate:
- evaluated the performance of the final system against the initial specification
 - produced initial specifications and final performance which agreed very closely.

N. Report

The report

- a. contains a clear account of most stages of the development of the project
 - b. adequately covers all stages of the development of the project
 - c. contains an acknowledgement of all sources of information and help.
-

18.3 Evidence to Support the Award of Marks

The development of the coursework project should be fully documented in the report which forms the basis for the assessment.

The report should be such that it would enable someone else to carry out the same work and to know what to expect in terms of the artefact's function and performance. It should be presented in a logical order that is easy to read and understand. It must contain:

- an acknowledgement of all sources of information and help;
- clear photographic evidence.

Marks should only be awarded when there is clear supporting evidence. Teachers are expected to annotate fully the reports of candidates to identify the relevant evidence.

The report must contain a completed Candidate Record Form and a Candidate Record of Supervision Form (Appendix C).

Supervision and Authentication

19.1 Supervision of Candidates' Work

Candidates' work for assessment must be undertaken under conditions which allow the teacher to supervise the work and enable the work to be authenticated. As much work as possible must be conducted in the centre under the direct supervision of the teacher. If it is necessary for some assessed work to be done outside the centre, sufficient work must take place under direct supervision to allow the teacher to authenticate each candidate's whole work with confidence.

19.2 Guidance by the Teacher

The work assessed must be solely that of the candidate concerned.

It is the teacher's task to ensure that appropriate project work is undertaken by the candidate and to provide the candidate with appropriate guidance. The supervisor should also provide additional guidance and assistance if requested but this must be taken into account when the work is assessed. The attention of teachers is drawn to the distinction between *guidance* and *assistance* given to candidates. When the supervisor gives advice to the candidate *but* does not become involved in doing the work, this is classed as *guidance*. When the teacher helps the candidate by becoming involved in doing the work, e.g. fault finding, this is classed as *assistance*.

19.3 Unfair Practice

At the start of the course, the supervising teacher is responsible for informing candidates of the AQA Regulations concerning malpractice. Candidates must not take part in any unfair practice in the preparation of coursework to be submitted for assessment, and must understand that to present material copied directly from books or other sources without acknowledgement will be regarded as deliberate deception. Centres must report suspected malpractice to AQA. The penalties for malpractice are set out in the AQA Regulations.

19.4 Authentication of Candidates' Work

Both the candidate (on the Candidate Record Form, Appendix C) and the teacher (on the Centre Declaration Sheet, Appendix C) are required to sign declarations confirming that the work submitted for assessment is the candidate's own. The teacher declares that the work was conducted under the specified conditions, and requires the teacher to record details of any additional assistance.

Standardisation

20.1 Annual Standardisation Meetings

Annual standardisation meetings will usually be held in the autumn term. Centres entering candidates for the first time must send a representative to the meetings. Attendance is also mandatory in the following cases:

- where there has been a serious misinterpretation of the specification requirements;
- where the nature of coursework tasks set by a centre has been inappropriate;
- where a significant adjustment has been made to a centre's marks in the previous year's examination.

Otherwise attendance is at the discretion of centres. At these meetings support will be provided for centres in the development of appropriate coursework tasks and assessment procedures.

20.2 Internal Standardisation of Marking

The centre is required to standardise the assessments across different teachers and teaching groups to ensure that all candidates at the centre have been judged against the same standards. If two or more teachers are involved in marking a component, one teacher must be designated as responsible for internal standardisation. Common pieces of work must be marked on a trial basis and differences between assessments discussed at a training session in which all teachers involved must participate. The teacher responsible for standardising the marking must ensure that the training includes the use of reference and archive materials such as work from a previous year or examples provided by AQA. The centre is required to send to the moderator a signed Centre Declaration Sheet (Appendix C) confirming that the marking of centre-assessed work at the centre has been standardised. If only one teacher has undertaken the marking, that person must sign this form.

Administrative Procedures

21.1 Recording Assessments

The candidates' work must be marked according to the assessment criteria set out in Section 18. Teachers should keep records of their assessments during the course in a form which facilitates the complete and accurate submission of the final overall assessments at the end of the course.

At the beginning of the course, centres must inform AQA on Form A (Early Information) of the approximate number of candidates to be entered so that appropriate documentation may be sent.

21.2 Submitting Marks and Sample Work for Moderation

The total component mark for each candidate must be submitted to AQA on the mark sheets provided or by Electronic Data Interchange (EDI) by the specified date. Centres will be informed which candidates' work is required in the samples to be submitted to the moderator.

21.3 Factors Affecting Individual Candidates

Teachers should be able to accommodate the occasional absence of candidates by ensuring that the opportunity is given for them to make up missed assessments.

Special consideration should be requested for candidates whose work has been affected by illness or other exceptional circumstances. Information about the procedure is issued separately. Details are available from AQA and centres should ask for a copy of: *Regulations and Guidance relating to Candidates with Particular Requirements*.

If work is lost, AQA should be notified immediately of the date of the loss, how it occurred, and who was responsible for the loss. AQA will advise on the procedures to be followed in such cases.

Where special help which goes beyond normal learning support is given, AQA must be informed so that such help can be taken into account when assessment and moderation take place.

Candidates who move from one centre to another during the course sometimes present a problem for a scheme of internal assessment. Possible courses of action depend on the stage at which the move takes place. If the move occurs early in the course the new centre should take responsibility for assessment. If it occurs late in the course it may be possible to accept the assessments made at the previous centre. Centres should contact AQA at the earliest possible stage for advice about appropriate arrangements in individual cases.

21.4 Retaining Evidence

The centre must retain the work of all candidates, with Candidate Record Forms (Appendix C) attached, under secure conditions, from the time it is assessed, to allow for the possibility of an enquiry upon result. The work may be returned to candidates after the issue of results provided that no enquiry upon result is to be made which will include re-moderation of the coursework component. If an enquiry upon result is to be made, the work must remain under secure conditions until requested by AQA.

Moderation

22.1 Moderation Procedures

Moderation of the coursework is by inspection of a sample of candidates' work, sent by post from the centre to a moderator appointed by AQA. The centre marks must be submitted to AQA and the sample of work must reach the moderator by 15 May in the year in which the qualification is awarded.

Following the re-marking of the sample work, the moderator's marks are compared with the centre marks to determine whether any adjustment is needed in order to bring the centre's assessments into line with standards generally. In some cases it may be necessary for the moderator to call for the work of other candidates. In order to meet this possible request, centres must have available the coursework and Candidate Record Form (Appendix C) of every candidate entered for the examination and be prepared to submit it on demand. Mark adjustments will normally preserve the centre's order of merit, but where major discrepancies are found, AQA reserves the right to alter the order of merit.

22.2 Post-Moderation Procedures

On publication of the GCE results, the centre is supplied with details of the final marks for the coursework component.

The candidates' work is returned to the centre after the examination with a report form from the moderator giving feedback to the centre on the appropriateness of the tasks set, the accuracy of the assessments made, and the reasons for any adjustments to the marks.

Some candidates' work may be retained by AQA for archive purposes.

Awarding and Reporting

23

Grading, Shelf-Life and Re-Sits

23.1 Qualification Titles	<p>The qualification based on these specifications have the following titles:</p> <p>AQA Advanced Subsidiary GCE in Electronics AQA Advanced Level GCE in Electronics</p>
23.2 Grading System	<p>Both the AS and the full A Level qualifications will be graded on a five-grade scale: A, B, C, D and E. Candidates who fail to reach the minimum standard for grade E will be recorded U (unclassified) and will not receive a qualification certificate.</p> <p>Individual assessment unit results will be certificated.</p>
23.3 Shelf-Life of Unit Results	<p>The shelf-life of individual unit results, prior to the award of the qualification, is limited only by the shelf-life of the specification.</p>
23.4 Assessment Unit Re-Sits	<p>Each assessment unit may be re-taken an unlimited number of times within the shelf-life of the specification. The best result will count towards the final award. Candidates who wish to repeat an award must enter for at least one of the contributing units and also enter for certification (cash-in). There is no facility to decline an award once it has been issued.</p>
23.5 Minimum Requirements	<p>Candidates will be graded on the basis of work submitted for the award of the qualification.</p>
23.6 Awarding and Reporting	<p>This Specification complies with the grading, awarding and certification requirements of the current GCSE, GCE, VCE and GNVQ Code of Practice 2006/2007, and will be revised in the light of any subsequent changes for future years.</p>

Appendices

A

Grade Descriptions

The following grade descriptors indicate the level of attainment characteristic of the given grade at A Level. They give a general indication of the required learning outcomes at each specific grade. The descriptors should be interpreted in relation to the content outlined in the specification; they are not designed to define that content.

The grade awarded will depend in practice upon the extent to which the candidate has met the assessment objectives (as in Section 6) overall. Shortcomings in some aspects of the examination may be balanced by better performances in others.

- Grade A** Candidates will demonstrate a thorough mastery of the underlying principles of the whole specification. They will have a clear and detailed knowledge of the subject content with only minor omissions in their understanding. Candidates will be able to apply their knowledge to solve problems that are set in unfamiliar situations. They will be able to recall standard circuit diagrams accurately and be able to suggest modifications to enable circuits to perform an amended function. In written papers, all questions will be attempted and answers will contain clear and detailed solutions, with descriptive answers being presented in a coherent and logical manner. Diagrams and graphs will be clearly labelled and drawn with precision. Answers to numerical questions will show some understanding of the underlying concepts with a logical progression to achieving the final solution. In coursework, candidates will have worked carefully from having initially identified a problem to be solved through specifying, constructing and testing the solution to producing a coherent and complete account of the work undertaken. In general, coursework will contain at least the minimum number of components suggested within the specification and will reflect an underlying grasp of the fundamental concepts associated with the project. Candidates will have received little or no guidance from the supervisor and will have worked safely and systematically. The final solution will be thoroughly tested and documented and the report will be logical, detailed and yet succinct.
- Grade C** Candidates will demonstrate an understanding of the underlying principles of much of the specification. They will have a clear and detailed knowledge of the subject content but with a number of omissions in their understanding. Candidates will be able to apply their knowledge to solve some problems that are set in unfamiliar situations though generally they will be unable to provide complete solutions. They will be able to recall most circuit diagrams accurately and attempt modifications to enable circuits to perform an amended function. In written papers, most questions will be attempted by the candidates and will contain reasonably detailed solutions, with descriptive answers, in general, being presented clearly. Diagrams and

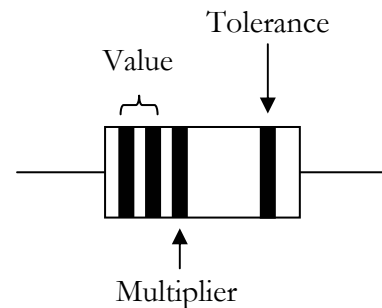
graphs will be neatly drawn and labelled. Answers to numerical questions will, in many cases, show knowledge of the underlying concepts, with progression towards achieving the final answer. Many answers will be accurate but there will be some omissions and errors. In coursework, the candidates will have worked carefully from having initially identified a problem to be solved, through specifying, constructing and testing the solution to producing a coherent and complete account of the work undertaken. In general, the coursework of this standard will contain at least the minimum number of components suggested within the specification and will sometimes have been followed through to a successful outcome. Candidates will often need guidance from the supervisor but will have worked safely and systematically throughout the project work. The final solution will be thoroughly tested and documented and the report will be reasonably detailed.

Grade E Candidates will have demonstrated that they have gained some understanding of the underlying principles from several parts of the specification. They will have some knowledge of the majority of the subject content but will demonstrate a detailed knowledge of only a few areas. Candidates will be able to recall standard circuit diagrams but will not be able to provide modifications to enable the circuit to perform amended functions. In written papers, many questions will be attempted by the candidates though detailed answers will be rare and descriptive answers will contain significant omissions and may lack clarity. Diagrams and graphs will contain some errors and lack detail. Numerical questions will be attempted, though calculations involving re-arrangement of formulae will often be unsuccessful. In coursework, candidates will have identified a problem to be solved but will have not given a detailed specification of the required outcome. Coursework will be basic and the candidates will have received guidance from their supervisor and may have needed assistance to ensure that the outcome was working. The testing and documentation of the final outcome will be superficial and there will be some significant omissions.

B**Data Sheet**

Resistors	Preferred values for resistors (E24) series: 1.0, 1.1, 1.2, 1.3, 1.5, 1.6, 1.8, 2.0, 2.2, 2.4, 2.7, 3.0, 3.3, 3.6, 3.9, 4.3, 4.7, 5.1, 5.6, 6.2, 6.8, 7.5, 8.2, 9.1 ohms and multiples of ten.
Resistor Printed Code (BS 1852)	This code consists of letters and numbers: R means $\times 1$ K means $\times 1000$ (i.e. 10^3) M means $\times 1\,000\,000$ (i.e. 10^6) Position of the letter gives the decimal point Tolerances are given by the letter at the end of the code, F = $\pm 1\%$, G = $\pm 2\%$, J = $\pm 5\%$, K = $\pm 10\%$, M = $\pm 20\%$.

Resistor Colour Code	Number	Colour
	0	Black
	1	Brown
	2	Red
	3	Orange
	4	Yellow
	5	Green
	6	Blue
	7	Violet
	8	Grey
	9	White



Tolerance, gold = $\pm 5\%$, silver = $\pm 10\%$, no band $\pm 20\%$.

Silicon diode	$V_F = 0.7\text{V}$	
Silicon transistor	$V_{be} \approx 0.7\text{V}$ in the on state $V_{ce} \approx 0.2\text{V}$ when saturated	
Resistance	$R_T = R_1 + R_2 + R_3$	series
	$\frac{1}{R_T} = \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}$	parallel
Capacitance	$\frac{1}{C_T} = \frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3}$	series
	$C_T = C_1 + C_2 + C_3$	parallel
Time constant	$T = CR$	

A.C. theory	$I_{\text{rms}} = \frac{I_o}{\sqrt{2}}$	
	$V_{\text{rms}} = \frac{V_o}{\sqrt{2}}$	
	$X_C = \frac{1}{2\pi fC}$	reactance
	$X_L = 2\pi fL$	reactance
	$f = \frac{1}{T}$	frequency, period
	$f_0 = \frac{1}{2\pi\sqrt{LC}}$	resonant frequency
Operational amplifier	$G_V = \frac{V_{\text{out}}}{V_{\text{in}}}$	voltage gain
	$G_V = -\frac{R_f}{R_1}$	inverting
	$G_V = 1 + \frac{R_f}{R_1}$	non-inverting
	$V_{\text{out}} = -R_f \left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \right)$	summing
Astable and Monostable using Nand Gates	$f \approx \frac{1}{2RC}$	astable
	$T \approx RC$	monostable
555 Astable and Monostable	$T = 1.1RC$	monostable
	$t_H = 0.7(R_A + R_B)C$ $t_L = 0.7R_B C$	astable
	$f = \frac{1.44}{(R_A + 2R_B)C}$	two resistor circuit
Electromagnetic Waves	$c = 3 \times 10^8 \text{ m s}^{-1}$	speed in vacuo
List of BASIC Commands	DIM variable [(subscripts)]	
	DO [{ WHILE UNTIL } condition] [statement block]	
	LOOP	
	DO [statement block]	
	LOOP [{ WHILE UNTIL } condition]	

FOR counter = start **TO** end [**STEP** increment]
 [statement block]
NEXT counter

GOSUB [label | line number]
 [statement block]
RETURN

IF condition **THEN**
 [statement block 1]
ELSE
 [statement block 2]

INKEYS

INP (port %)

INPUT [;] [“prompt” { ; 1 , }] variable list (comma separated)

LPRINT [expression list] [{ ; 1 , }]

OUT port%, data%

PRINT [expression list] [{ ; 1 , }]

REM remark

The Candidate Record Forms have been deleted from this specification because of changed requirements. The latest version of the forms are on the [Coursework Administration](#) pages of the Website.

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Overlaps with other Qualifications

The AQA GCE Electronics Specification overlaps peripherally with AQA GCE Physics through the Physics optional module 9, Electronics. There is marginal overlap with AQA GCE Design and Technology. There is no significant overlap with GCE ICT.

In the case of GNVQ Engineering there is some overlap between unit 2 and GCE Electronics; there is marginal overlap with units 4 and 12 and substantial overlap with units 8, 13 and 14. There is no significant overlap with AVCE Science: Manufacturing.

The overlap with AQA GCE Mathematics A and B rests only on the use and application of certain formulae and equations. There is no overlap with either AQA GCE Biology A and B and Chemistry.